METHOD 1039.4

BURN-IN (FOR TRANSISTORS)

1. Purpose. This test is performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the semiconductor device at specified conditions to reveal electrical failure modes that are time and stress dependent.

2. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein. Preburn-in measurements shall be made as applicable. The failure criteria shall be as specified.

2.1 Mounting. Devices with leads projecting from the body shall be mounted by their leads at least .250 inch (6.35 mm) from the seating plane. Unless otherwise specified, devices with studs or case shall be mounted by the stud or case.

2.1.1 Test condition A, steady-state reverse bias. The transistor primary blocking junction, as specified, shall be reverse biased for 48 hours minimum, except PNP bipolar transistors shall be 24 hours, at the ambient temperature specified (normally +150°C) and at 80 percent of its maximum rated collector-base voltage. For bipolar transistors, the V_{CB} base is not to exceed the maximum collector-emitter voltage rating. For field-effect (signal or low power) transistors, the gate to source voltage, with drain to source shorted, shall be as specified. At the end of the high-temperature test time, specified herein, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until T_C = +30°C ±5°C is attained. After room ambient temperature has been established, the bias voltage shall be removed. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post burn-in reverse-current measurement(s). Unless otherwise specified, after burn-in voltage is removed, post burn-in measurements shall be completed within 24 hours. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

2.1.2 Test condition B, steady-state power. All devices shall be operated at the maximum rated power related to the test temperature for 160 hours minimum at the specified test conditions (excluding microwave).

a. For bipolar transistors, the temperature and power shall be specified. Unless otherwise specified, the temperature shall be as follows:

   T_A = room ambient as defined in the general requirements, 4.5 herein. for small signal, switching, and medium power devices intended for printed circuit board mounting; T_J = maximum rated temperature, +0°C, -25°C, for devices intended for chassis or heat sink mounting. Case temperature burn-in at maximum ratings (typically T_C = +100°C) may be substituted on the chassis or heat sink mounted devices at the supplier's option. If the voltage conditions specified herein cause the SOA rating to be exceeded, then the voltage shall be decreased until the SOA rating is met while maintaining the full rated power condition. For microwave bipolar transistors, the temperature, voltage, and current shall be as specified in the detail specification.

b. For unijunction and field-effect (signal and low power) transistors, the temperature, voltage, and current shall be as specified.

c. Post burn-in measurements shall be as specified.

d. Unless otherwise specified, post burn-in readings shall be taken within 96 hours. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

3. Summary. Test condition letter and the following conditions shall be specified in the detail specification.

3.1 Test condition A:

a. Junction to be reverse biased (see 2.1.1).

b. Gate to source voltage for FETs (see 2.1.1).

c. Test temperature (see 2.1.1).

d. Test time for FETs (see 2.1.1).

e. Voltage for post burn-in reverse current measurement (see 2.1.1).

f. Time for completion of post burn-in measurements, if other than 24 hours (see 2.1.1).

g. Criteria for failure (see 2.).

3.2 Test condition B:

a. Test temperature, if other than as specified in 2.1.2.

b. Test conditions (see 2.1.2).

c. Power for bipolar transistors (see 2.1.2).

d. Voltage and current for unijunction and FETs (see 2.1.2).

e. Preburn-in and post burn-in measurements (see 2.1.2).

f. Time for completion of post burn-in measurements, if other than as specified in 2.1.2.

g. Criteria for failure (see 2.).